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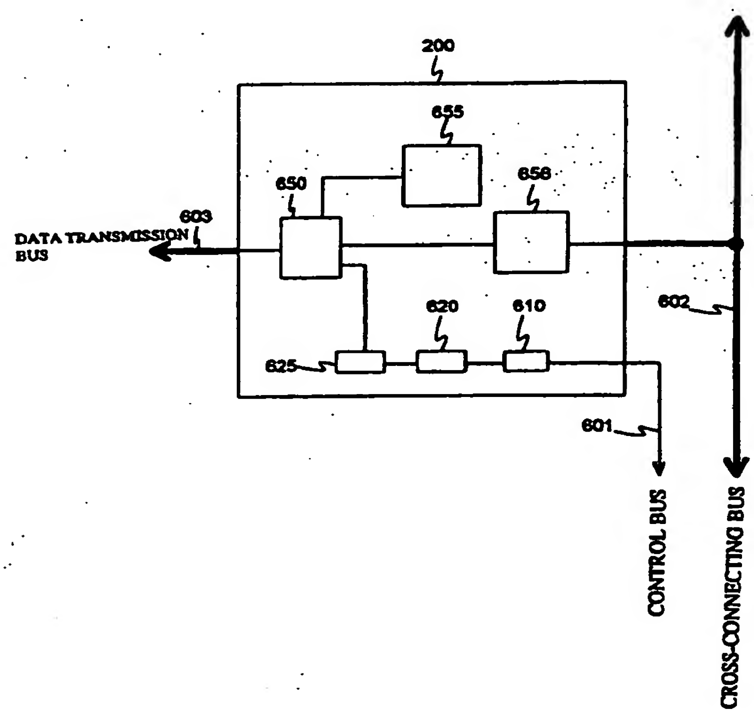
(57) Abstract

The invention relates to the remote control of communications equipment, in particular to the way in which remote control data are included in a data stream communicated by a communications device. The idea of the invention is to utilize existing cross-connecting structures found in a cross-connecting circuit in the transmission of a control channel. The cross-connecting circuit according to the invention uses individual switching definition for each bit. In the cross-connecting circuit according to the invention the control channel data can be included in the outgoing data stream using a special bit-specific instruction which connects one bit from an internal intermediate register in the circuit. Since the instruction is bit-specific, the control channel capacity can in principle be any number of bits.



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Method and apparatus for including control channels in a data stream

The invention relates to remote control of communications equipment, especially to the manner in which remote control data are included in a data stream.

Fig. 1a shows a base station network in a cellular radio system, comprising a base station controller 100 (BSC) and a plurality of base transceiver stations 101 (BTS). The base station controller 100 is further connected to a mobile switching center, which is not shown. To enable transmission of data between them, the base station controller 100 and base transceiver stations 101 are interlinked through a plurality of connections which constitute a so-called transmission system in the base station network. The standards for a cellular radio system such as the Global System for Mobile Telecommunications (GSM), for example, usually do not specify the transmission method to be used in the base station network, except for defining the functions that the transmission method has to be capable to realize. In GSM, the interface between two base transceiver stations or a base transceiver station and the base station controller, as defined in the standards, is called the Abis interface. The transmission method may comprise e.g. a 2-Mbps or 1.5-Mbps PCM connection (Pulse Coded Modulation; ITU-T G.703 and G.704), SDH connection (Synchronous Digital Hierarchy; ITU-T G.774.03), ATM connection (Asynchronous Transfer Mode; ETS 300 371), ISDN connection (Integrated Services Digital Network), or a HDSL connection (High Density Digital Subscriber Line). The physical connection may comprise a conventional copper wire, optical cable or a microwave radio link.

In the base transceiver stations and base station controller of the system depicted in Fig. 1a connection to the transmission system is realized through a cross-connect 102. A cross-connect 102 in a base transceiver station may comprise one or more transmission units (TRU). Cross-connecting means that the incoming data, which are arranged in frames, can be connected to the outgoing direction in the cross-connecting device such that the location of the data bits in the frames can be altered. The base transceiver station cross-connect "drops" certain bits and time slots in the transmission system frame to the base transceiver station, i.e. directs data concerning that particular base transceiver station, which arrive in certain time slots, to the base transceiver station and, on the other hand, associates the data leaving the base transceiver station in the direction of the base station controller with certain time slots allocated to that base transceiver station. The cross-connect may also perform summing, multiplication or other operations on the incoming data before the data are connected to the outgoing direction. When the cross-connect is placed

either in the same equipment rack with the base transceiver station or in its immediate vicinity, the base transceiver station constitutes a compact unit and the base station network can be easily modified and expanded.

The transmission capacity allocated to one base transceiver station depends on how many TRX (Transmit/Receive) units 103 it contains. The TRXs constitute a radio interface to terminal equipment 104, and the number of TRX units determines how many simultaneous speech or data connections the base transceiver station can handle. Different parts of the base station network may also require different amounts of transmission capacity depending on the base station network topology. In a tree-like base station network the highest capacity is required of connections near to the base station controller.

At its simplest a transmission system comprises a so-called point-to-point connection where a given GSM base transceiver station communicates directly with the base station controller and through the latter with a switching center. However, in the case of a 2-Mbps PCM, for example, the traffic capacity required by a base transceiver station having one TRX is quite small compared to the whole transmission band. Typically, two and a half time slots in a PCM frame (6 to 8 voice channels and signalling), or 160 kbps, are reserved for one TRX. Therefore, a point-to-point connection often wastes capacity and becomes expensive. On the other hand, the use of existing ISDN connections for point-to-point connections may be an alluring idea. Network duplication can be realized using redundant point-to-point connections.

The transmission band can be utilized more efficiently by chaining base transceiver stations (so-called multidrop chain structure). In the chain, several base transceiver stations share, on a time division basis, the same transmission medium, thus better utilizing the connection capacity. Thus the integrated cross-connecting function in the base transceiver station really becomes useful as the time slot arrangements can be made within the base transceiver station itself.

Loop networks are used for network duplication. Base transceiver stations are looped together so that there exists at all times a transmission connection in both directions of the loop from each base transceiver station to the BSC. Normally, one of the connections is active. Network monitoring is realized using status bits, or so-called pilot bits, which each base transceiver station sends in both transmission directions in the loop. A change in the state of a pilot bit indicates a network fault, at which point cross-connects in base transceiver stations switch over to the back-up

connection. Network synchronization data are also sent using status bits of their own. A switch-over as quick as possible enables network operation without disconnected calls even in fault situations. A GSM call can tolerate a 500-ms break in the transmission connection without disconnecting the call proper.

Fig. 1b shows a prior-art cross-connect in a GSM base transceiver station. It has two separate transmission units 110 and 111. Both transmission units have an "outbound" Abis interface according to the GSM standards, i.e. an interface to either the base station controller or another base transceiver station (not shown). In addition, both transmission units have an operation and maintenance connection to the base station controller. One of the transmission units is also connected to the internal data bus in the base transceiver station which is used in sending the downlink data associated with the voice and signalling connections handled by the base transceiver station to the TRX units (not shown) of the base transceiver station, and, correspondingly, the uplink data from the TRX units to the base station controller. In the prior-art implementation the transmission units 110 and 111 in the cross-connect are wholly separate and they both have internal cross-connecting buses of their own. The transmission units are interconnected through the Abis interface as shown in Fig. 1b.

In future cellular radio systems the average cell size will be smaller and, hence, the number of cells greater than today so that transmission systems shall be capable of handling more base transceiver stations, and network topologies and cross-connections will be more complex than now. The operator providing the transmission medium will not necessarily be the same as the operator running the cellular radio system, so the latter must be able to realize transmission between base transceiver stations and base station controllers as advantageously and efficiently as possible, using the various transmission possibilities available.

Ordinarily, a base station comprises a base control functions (BCF) unit which controls the operation of the TRX and TRU units within the base station. It involves, among other things, the specification of radio path parameters, allocation of time slots and configuration of the transmission unit. In addition, the BCF gathers base station fault information in a centralized fashion.

Some transmission devices employ a special asynchronous operation and maintenance channel which typically has a transmission rate of 1200 to 9600 bps. Such a channel is hereinafter called a control channel. In GSM base stations the operation and maintenance function for the base station's transmission equipment, i.e. TRU

units, can be realized separately from the GSM operation and maintenance by means of a control channel. An operation and maintenance connection can be established locally direct to a transmission device or an asynchronous control channel may be sampled into the transmission stream at the far end. In the latter case, the TRU unit decodes the control messages from the transmission interface time slots and sends information to the far end in the reverse manner. The fact that the transmission O&M and GSM O&M are separate is significant e.g. in a situation where the GSM transmission network is part of the public telephone network and e.g. leased lines are used, in which case the GSM operator and the transmission operator may not be the same.

A conventional way of realizing the control channel extraction from the transmission stream and inclusion into the transmission stream is to have a separate encoder/decoder block at the transmission device input: e.g. in the framer circuit or in the cross-connecting circuit prior to the cross-connect part or using a separate circuit between said circuits. Commercial framer circuits typically do not have this feature. A dedicated circuit for this purpose, on the other hand, is an expensive solution.

A control channel encoder/decoder can be realized in the cross-connecting circuit using a special intermediate register. In the conventional case of control channel coding the intermediate register is filled once in every frame with values sampled from the control channel, after which the process waits for a suitable frame phase, whereafter the register is emptied into the data stream. This requires time slot counters and bit counters, among other things, the implementation of which reserves logic elements in the circuit used.

An object of the invention is to provide a system with which a control channel can be included in a data stream sent out from a transmission device. Another object of the invention is to provide such a system in such a manner that it uses as few as possible of the logic elements of the microcircuit used in the implementation.

The objects are achieved by implementing the cross-connecting block in a transmission device such that it can use the intermediate register as a data source, so that in response to a certain cross-connecting instruction the cross-connecting block reads from the intermediate register at least one bit and places it into the outgoing data stream.

The cross-connecting system according to the invention is characterized in that in response to a certain cross-connecting instruction the cross-connecting system adds at least one register bit to a data stream cross-connected to a data transmission bus.

The invention also pertains to a method which comprises steps in which
said control signal is sampled and
in response to a certain cross-connecting instruction the cross-connecting element in the cross-connecting system adds at least one sample bit to said outgoing data stream.

The invention further pertains to a base station characterized in that a cross-connecting system, which there is at least one in the base station, is configured to add, in response to a certain cross-connecting instruction, at least one register bit to a data stream cross-connected to an external data transmission bus.

The idea of the invention is to utilize existing cross-connecting structures in a cross-connecting circuit in the transmission of a control channel. The cross-connecting circuit according to the invention defines the switching individually for each bit. In the cross-connecting circuit according to the invention, the control channel information can be included in the outgoing data stream with a special bit-specific instruction which shifts out one bit from an internal intermediate register in the circuit. Since the instruction is bit-specific, the capacity of the control channel can in principle be set to any number of bits.

The invention will now be described in more detail with reference to the preferred embodiments presented by way of example and to the accompanying drawings in which

Fig. 1a	depicts a known base station network,
Fig. 1b	depicts a known cross-connect for a base station,
Fig. 2	depicts the structure of a base station according to an embodiment of the invention,
Fig. 3	depicts the structure of a transmission unit according to an embodiment of the invention,
Fig. 4	depicts the structure of a common part,
Fig. 5	depicts the arrangement of instruction words in the control memory,
Fig. 6	depicts the structure of a preferred embodiment of the invention, and
Fig. 7	depicts the operation according to a preferred embodiment of the invention.

Like elements in the drawings are denoted by like reference designators.

In the inventional structural solution the cross-connection and the functions required by the transmission connections are implemented modularly by decentralizing them into several parts which in this patent application are called transmission units. Decentralization is to be understood such that a single transmission unit can establish all transmission connections of a base transceiver station but units can be added according to capacity requirements so that they function as a whole. The cross-connection is shared by the transmission units through a parallel bus in the so-called motherboard, which bus interconnects the transmission units and is advantageously duplicated for added reliability. From the base station control perspective the transmission units constitute one manageable whole. Each transmission unit realizes a certain type of standard transmission interface.

As the amount of GSM traffic increases there also emerges a need to have different transmission interfaces in one and the same base transceiver station. Therefore, the new base station solution can use transmission units of many different types. Within a transmission unit, a given first part realizes the transmission interface and converts the received data, which are to be cross-connected, from the format used in the transmission system to the internal format used in the cross-connect. The data are written in that latter format to the cross-connecting bus interconnecting the transmission units. The other parts of the transmission unit realize advantageously at least cross-connection, unit control, synchronization with other transmission units and interfaces to the base station motherboard. A transmission unit may comprise one or more printed circuit boards. Hereinafter, the term "special part" refers to parts realizing a transmission interface and the term "common part" refers to the cross-connecting and bus interface block. In addition to the functions mentioned above, a transmission unit may include other functional blocks, too.

The special part in the transmission unit adapts the cross-connect in the base transceiver station to the base station network's transmission system, which may be a PCM, HDSL or an ISDN system, for example. Advantageously the special part may also comprise adapter circuits for different physical transmission media such as copper wire, optical cable or radio link.

Fig. 2 shows an example of the new structure for the cross-connect in a base transceiver station. The cross-connect comprises at least one transmission unit 200. It may also have more transmission units depending on the desired quality and

quantity of the transmission connections. Each transmission unit 200 comprises a common part 202 and special part 204. In a preferred embodiment each transmission unit is realized on a circuit board containing the necessary physical interfaces and functional blocks required by the common part 202 and special part 204. The transmission units are electrically coupled to the internal doubled cross-connecting bus of the base transceiver station. The transmission units may also be coupled to the data bus used by the transmitter/receiver units, or TRXs, of the base transceiver station. In a typical embodiment, where the TRX units of the base transceiver station are connected to the data bus, at least one transmission unit has to be coupled to the data bus to enable data communications between the TRX units and transmission connections outside the base transceiver station via the transmission units. In other embodiments of the invention the TRX units may also be coupled to the cross-connecting bus.

In addition to the cross-connecting bus and data bus shown in Fig. 2 the base transceiver station may also include other buses for controlling and synchronizing the operation of the transmission units. In such an embodiment the transmission units are coupled to those buses, too.

The special part 204 in each transmission unit 200 has at least one bi-directional external transmission connection 206 which may be e.g. a PCM, SDH, ATM, ISDN, HDSL or some other connection. The special part, which is of RRI (Radio Relay Interface) type, is advantageously directly connected to the outside unit of the microwave radio in the base transceiver station. In one cross-connect the external transmission connections in the special parts of the transmission units may all be identical or they may be different. In addition, a transmission unit may have interfaces for two or more types of transmission connections. Data traffic between the special part 204 and common part 202 is preferably substantially similar in all transmission units independent of the type of the external transmission connection. An advantageous solution is to provide N standard-capacity (say, 2.048 Mbps) connections between the special part and common part, where N is chosen such that the transmission capacity between the special part and common part at least equals the combined capacities of the transmission connections coupled to the special part.

Fig. 3 shows in more detail a special part 300 of a transmission unit in a cross-connect according to the invention, which special part is intended for the transmission and reception of a PCM signal. It has an N-channel line interface circuit 301 which, when receiving, is adapted to the received signal level and extracts and regenerates timing information from the data. Depending on the application, the line

impedance may be 75 ohms, 120 ohms (E1) or 100 ohms (T1). When transmitting, the line interface circuit 301 adapts the data to the transmission medium, which is a coaxial cable or twisted-wire pair. The transmission line is logically terminated by an N-channel framer circuit 303. When receiving, it decodes the line coding (e.g. high density bipolar 3, HDB3; alternate mark inversion, AMI; or binary 8 zero substitution, B8ZS) and becomes locked to the frame phase by means of frame alignment words in the data stream. In addition, the framer circuit 303 includes other functions e.g. for processing overhead data; decoding the channel signalling, handling of T1 HDLC messages, processing various alarm information, etc. Finally, the special part delivers the data stream to the common part in a form in which the clock signal is separate from the data and the start of a frame is indicated using a signal of its own. In the outgoing direction the steps mentioned above are performed in the reverse order.

Regardless of whether the transmission interface capacity is 2.048 Mbps (E1) or 1.554 Mbps (T1), the framer circuit 303 always provides an N x 2.048 Mbps interface to the common part. This is achieved by internal data buffering inside the framer circuit 303 and by placing the data in the E1 frame structure in connections between the framer circuit 303 and common part 202, so that if the lower-capacity T1 frame structure is used in the transmission, the "extra" time slots in the E1 frame structure are filled with pseudo-data. The same principle holds with other applications of the special part; the interface to the common part is always N x 2.048 Mbps.

Fig. 4 shows in simplified form the basic electrical structure of a transmission unit's common part 202. The common part comprises a cross-connecting circuit 231, which usually is an application specific integrated circuit (ASIC) and which hereinafter will be called a switching circuit. In addition, the common part comprises an oscillator 232, microprocessor 233 and a cross-connecting bus interface 234. Transmitter and receiver blocks 235a and 235b for communications with the special part are located in the switching circuit 231 which further comprises, among other things, a cross-connecting processor 236, data memory (DM) 237 and control memory (CM) 238. The data memory 237 serves as an intermediate data store where the outgoing data, i.e. data flowing from the cross-connecting bus to transmitter blocks via the switching circuit, are temporarily stored for rearrangement. The microprocessor 233 controls the operation of the entire common part.

Through the cross-connecting bus interface 234 the common part is connected to the cross-connect's cross-connecting bus whose data structure conforms to a certain bus

protocol. Data on the cross-connecting bus are arranged in frames having a certain regular form. Each frame on the cross-connecting bus is stored in its turn to the data memory DM of the cross-connecting circuit 231. A cross-connecting processor XC reads data from the data memory DM e.g. one byte at a time and writes those data to transmitter blocks 235a which lead to the special part of the transmission unit. A term called granularity defines the smallest amount of data that can be independently managed in a write operation. If the granularity is one bit, it means that each bit read from the data memory DM and written to transmitter blocks 235a can be controlled independent of other bits. Instruction words read from the control memory CM determine the order in which the data read from the data memory DM are written to transmitter blocks 235a.

A GSM call according to the prior art reserves a 16-kbps capacity in the transmission system, corresponding to two bits in a PCM transmission system frame (according to G.703 and G.704 standards, PCM frames are repeated 8000 times a second in the transmission system so that one bit per frame corresponds to a capacity of 8 kbps). However, in the cross-connect according to the invention it is advantageous to prepare for the so-called half-rate GSM connections, each of which represents a transmission capacity of just 8 kbps. Since cross-connects have to be able to handle these connections independent of each other and, furthermore, since it is advantageous to prepare for the channel associated signalling (CAS) according to standards G.703 and G.704 in cross-connects, the granularity has to be one bit.

An essential component in the common part is the switching circuit, advantageously a special cross-connecting processor, which reads cross-connection data from the parallel bus linking the transmission units and directs said data in a certain order to the transmitter interfaces interconnecting the common part and special part wherefrom the data are further sent to the transmission system. To control the operation of the cross-connecting processor the common part has a control memory which contains instruction words.

To make it easier to understand the invention it will be next briefly described how the reading of the control memory affects in general the operation of the cross-connecting processor and how the data are arranged in the data memory.

The cross-connecting processor reads the control memory cyclically in step with the outgoing frame phase. The content of each instruction read from the control memory is interpreted, i.e. the type of the instruction is determined. Depending on the switching type specified by the instruction, data memory is read at one or more

memory locations indicated by the control word. The reading of control and data memory is advantageously realized in a "pipeline" fashion, i.e. as the data indicated by the previous instruction are read from the data memory, a new instruction word is already at the same time being read from the control memory. Various operations are possibly performed on the data read from the data memory, whereafter the data are taken in parallel form to the switching circuit's transmitter blocks.

The data in the data memory DM come from the cross-connecting bus which uses a certain frame structure. According to a preferred embodiment the cross-connecting bus frame comprises 54 blocks. Each block comprises 32 time slots and each time slot comprises eight bits. To avoid overlapping read and write operations the data memory comprises two identical one-frame halves so that the cross-connecting processor reads data from a frame stored in one half while at the same time the next frame from the cross-connecting bus is being written to the other half.

An instruction read from the control memory comprises parts so that a first part indicates to the cross-connecting processor the instruction type, a second part indicates the data memory block from where the cross-connecting processor has to read data this time, a third part specifies a time slot in the block, and a fourth part specifies a bit in the time slot. In an embodiment that has proven advantageous the instruction type is indicated using the two most significant bits of the 16-bit instruction word, the block is indicated using the next six most significant bits, the time slot is indicated using the next five most significant bits, and the bit is indicated using the three least significant bits. Since the six bits used for indicating the block could indicate up to 64 blocks and the preferred cross-connecting bus frame structure only comprises 54 blocks, the extra block numbers can be used to create instruction words that define operations which are not directed directly to any block in the data memory.

The address of the instruction word, i.e. its location in the control memory, indicates the transmitter block (i.e. transmitter interface) and its time slot which are affected by the operation defined by the instruction word and also the running number of the instruction word in the sequence of instruction words directed to that time slot. As the cross-connecting processor sequentially reads instruction words from the control memory, it directs the operations defined by the instruction words to each transmitter block in its turn. More detailed information about the use of the control memory and structure of instruction words is disclosed in patent application "Instruction architecture of cross-connecting processor" filed at the same time with this patent application by the same applicant.

Fig. 5 shows an advantageous way of arranging instruction words in the control memory 238. The purpose of the control memory is to hold the necessary control information, i.e. instructions comprised of one or more instruction words, which is needed for making the connection in the outgoing direction. The switching circuit control memory is preferably comprised of 16-bit-wide static RAM and has two switching tables (table 0 and table 1) per each of the circuit's eight 2-Mbps transmitter interfaces. Each table contains so much space that, if necessary, an individual connection can be specified for each bit in the E1 frame formed by the transmitter interface, i.e. 256 control words per table. If the switching circuit has, say, eight transmitter interfaces, the total size of the memory needed is 8 interfaces x 2 tables per interface x 256 instruction words per table x 16 bits per word = 65,536 bits.

The basic case is that each bit to be connected is defined separately, i.e. by an instruction of its own, comprising one instruction word. So, the control memory contains control words needed for making the connections. These instructions can be used to make all possible connections supported by the circuit.

In the solution according to the invention, the intermediate register containing control channel information is shifted out by one bit in response to a certain cross-connecting instruction, and that bit is added to the outgoing data stream in accordance with that particular cross-connecting instruction. Such cross-connecting instructions can be defined more than one among the cross-connecting instructions, depending on the number of bits in the intermediate register.

In a preferred embodiment of the invention the information on a continuous asynchronous control channel is included in the outgoing data stream as follows. Continuous control channel data are sampled continuously at a desired clock frequency according to the number of bits reserved for the channel embedded in the transmission stream. For example, if the channel capacity is 2 bits, the corresponding sampling rate is 16 kHz when a frame is repeated 8000 times a second. Sampled data are loaded in serial form into a SIPO-type (Serial In Parallel Out) shift register. Once per frame the contents of the register are loaded into a second shift register, which this time is a PISO-type (Parallel In Serial Out) register. This second shift register serves as the intermediate register described above, so data are shifted out of the shift register one bit at a time always when the cross-connecting processor in the circuit detects that the data source defined in the current cross-connecting instruction is the shift register containing control data. If the number of cross-connecting instructions of the type in question exactly matches the quantity required by the sampling rate selected, the shift register is fully emptied during one frame

and all sampled values are connected to the outgoing data stream. As this example shows, the intermediate register may be a combination of two registers, where one register can be filled with sampled data at the same time that data are being written out of the other register.

In practice, the sampling of data from the continuous signal into the intermediate register limits the channel capacity to certain values. For example, for frames repeated 8000 times a second the sampling rates and the corresponding bit quantities are as follows:

Sampling rate	*Number of bits*
8 kHz	1 bit
16 kHz	2 bits
32 kHz	4 bits
64 kHz	8 bits

So, the channel capacity is determined according to the sampling rate selected. The location of the channel in the outgoing data stream is determined according to the location of the cross-connecting instructions in the cross-connecting memory. Thus, the control channel can be located anywhere in the outgoing data stream frame.

A control channel transported in the frame structure across the transmission path is here called an embedded operation channel, EOC. In a preferred embodiment of the inventional system the EOC is handled by a switching circuit, more specifically a special EOC block in the switching circuit. Control channels are preferably handled separately in each of the eight 2-Mbps interfaces in the switching circuit, so the time slot and bit definitions of the EOCs in each interface can be made individually for each interface. For example, in an embodiment where the interfaces are E1 signal interfaces, any successive 1, 2, 4 or 8 bits in any one time slot can be defined as the EOC in the interface in question. In addition, 1, 2 or 4 bits of the Sa bits in time slot 0 can also be used for transporting the EOC. Possible bit rates in such an embodiment thus include 4 kbps, 8 kbps, 16 kbps, 32 kbps and 64 kbps.

Fig. 6 depicts functional blocks in a transmission unit 200 according to a preferred embodiment of the invention. The transmission unit is coupled to a control bus 601 and cross-connecting bus 602. The transmission unit comprises a sampling block 610 which continuously samples the signal on the control bus 601 at a predetermined sampling rate. Signal samples produced by the sampling block 610 are

stored in a first shift register 620. The sampling block 610 samples the control bus 601 continuously so that the samples taken during a given frame are transported into a second shift register 625 at the beginning of the next frame and the samples transported are cross-connected during the next frame in accordance with the cross-connecting instructions. A data memory 656 reads the cross-connecting bus 602 one frame at a time. Once a frame has been read, the samples stored in the first shift register 620 are transported into the second shift register 625. After that, the cross-connecting processor 650 executes the cross-connecting instructions in the cross-connecting instruction memory 655 and connects bits of the frame read from the data memory as well as control signal sample bits from the second shift register to a data transmission bus 603 in accordance with the cross-connecting instructions.

Fig. 7 illustrates the method realized by a transmission unit 200 according to the preferred embodiment of the invention depicted in Fig. 6. For simplicity, Fig. 7 does not show the sampling of the control bus. First, a new frame is read 710 from the cross-connecting bus and the control bus signal samples stored in a first shift register are transported 720 into a second shift register. Next, the cross-connecting processor reads 730 the next instruction from the cross-connecting instruction memory. If the cross-connecting instruction involves data read from the cross-connecting bus, stored in the data memory, the cross-connecting processor reads 741 the bit in question from the cross-connecting memory and writes 742 it to the outgoing data stream. If the cross-connecting instruction involves data in the second shift register, the cross-connecting processor reads 751 the next bit from said second shift register and writes 752 it to the outgoing data stream. After these steps it is checked 760 whether this cross-connecting instruction was the last one. If it was the last one, the process returns to the read next frame step 710. If the instruction was not the last one, the process returns to the read next instruction step 730.

The examples of Figs. 6 and 7 indicate that cross-connecting instructions process the cross-connection data one bit at a time. However, this does not limit the applications of the invention in any way, but cross-connection data can be processed in blocks of other sizes, too, e.g. in groups of several bits or in bytes.

In a transmission system according to the invention which comprises more than one transmission unit, the asynchronous control buses in the units are advantageously arranged in a tree-like network. The transmission units in the system form the control bus network nodes. The control bus network advantageously is a master-slave network in which only one unit at a time sends messages over the network. In master-slave communications, the master unit on top of the network sends an

addressed message on a channel. At each node the channel is branched down such that in the end the message reaches all units in the network. Only the slave unit that recognizes its address answers. The answer is summed into one channel with the output signals of all the other slave units. Since the other slave units stay silent, the answer reaches the master unit. So, with the summing method, one transmission channel per direction is enough for the master-slave communications of the whole network. In summing switching, the desired incoming channels are summed and the result of the summing is sent forward to the next node.

Thus, the data sampled into the shift registers may be the sum of multiple O&M or other control channels. Other possible control channels and signal sources may also be added to the sampled data. For example, the transmission unit described above may receive EOCs from one or more of said eight 2-Mbps signal interfaces. Such incoming EOCs can advantageously be combined in parallel form as well, i.e. the received EOC bits can be summed with the bits in the sampled data. The result can be included in the outgoing data stream in accordance with special cross-connecting instructions as described above.

In the embodiments described above the outgoing data stream is one of the 2-Mbps buses in the transmission unit described above. In a preferred embodiment of the invention, the outgoing data stream may also be the cross-connecting bus of the above-described transmission unit or similar system, so that the cross-connecting element connects intermediate register bits to the cross-connecting bus in accordance with cross-connecting instructions. Such an embodiment finds particular utility in a situation where the cross-connecting unit which is coupled to the cross-connecting bus and which receives the control bus is not the same as the cross-connecting unit which is coupled to the data transmission line in whose data stream the control bus data are to be included. In that case, the cross-connecting unit which receives the control bus connects the control bus data to certain time slots of the cross-connecting bus so that the cross-connecting unit coupled to said data transmission line connects these data to the data transmission line just as the other time slots.

The control bus can be communicated from a first transmission unit to a second transmission unit and therefrom to an external data transmission line also through a separate universal bus. In such an embodiment a transmission unit does not need functional blocks that enable the adding of the control bus to the data stream going to the cross-connecting bus. By means of a separate universal bus the control bus can be communicated independent of the cross-connecting bus to the second trans-

mission unit which adds it to the data stream going to the external data transmission line in the manner described above.

The method according to the invention enables the adding of control channel information to an outgoing data stream in a manner which is simpler than those used in the prior art and uses less logic elements than in the prior art.

Above a transmission unit was described as an advantageous application of the invention. However, the invention is not limited to transmission units but the control channel adding method according to the invention can be utilized in other cross-connects, too, which are controlled by means of a separate control channel.

Above the invention was described with reference to preferred embodiments, but it is obvious that the invention can be modified in many different ways according to the inventional idea defined by the claims set forth below.

Claims

1. A cross-connecting system for cross-connecting information coming from a first data transmission bus
to a second data transmission bus,
which system is arranged so as to receive information from a control bus of the cross-connecting system,
and which system comprises a register for storing the information coming from said control bus,
characterized in that the cross-connecting system is arranged so as to add, in response to a certain cross-connecting instruction, at least one bit in said register to a data stream cross-connected to the second data transmission bus.

2. The cross-connecting system of claim 1, **characterized** in that it is arranged so as to store information from said control bus by sampling the signal containing the information from said control bus and by storing the samples in said register.

3. A method for adding a control signal of a cross-connecting system
to an outgoing data stream of the cross-connecting system,
characterized in that it comprises steps in which
said control signal is sampled, and
in response to a certain cross-connecting instruction the cross-connecting element in the cross-connecting system adds at least one sample bit to said outgoing data stream.

4. A base station which comprises a cross-connecting bus and at least one cross-connecting system for switching information between an external data transmission bus and an internal cross-connecting bus in the base station wherein said at least one cross-connecting system comprises a register to store information coming from said control bus,
and in addition to which the base station comprises a control bus in the cross-connecting system and said cross-connecting system is arranged so as to receive information from the control bus in the cross-connecting system,
characterized in that said at least one cross-connecting system is arranged so as to add, in response to a certain cross-connecting instruction, at least one bit in said register to a data stream cross-connected to said external data transmission bus.

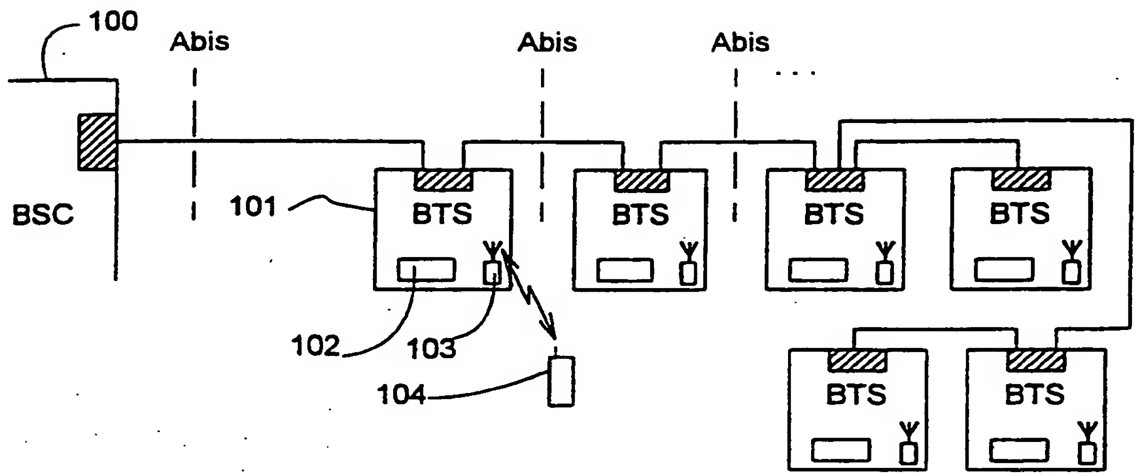

Fig. 1a
PRIOR ART

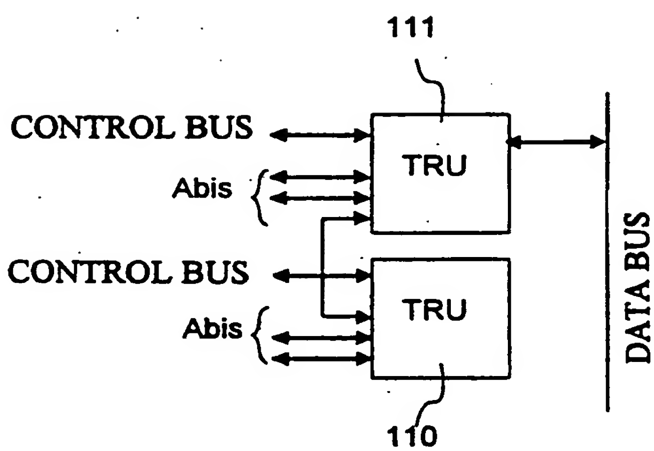

Fig. 1b
PRIOR ART

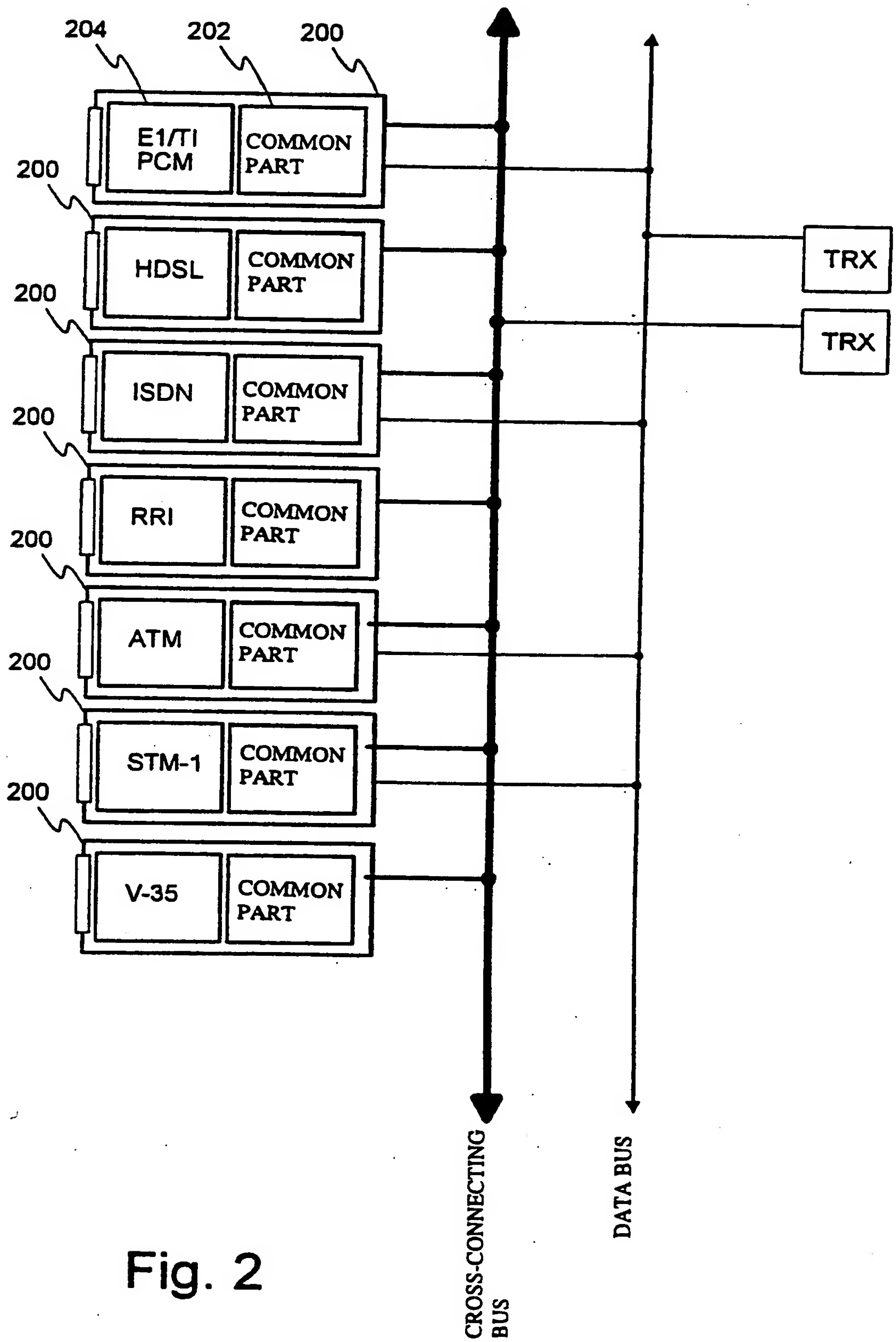
204
202
200
E1/TI PCM
COMMON PART
200
HDSL
COMMON PART
200
ISDN
COMMON PART
200
RRI
COMMON PART
200
ATM
COMMON PART
200
STM-1
COMMON PART
200
V-35
COMMON PART
TRX
TRX
CROSS-CONNECTING BUS
DATA BUS

Fig. 2

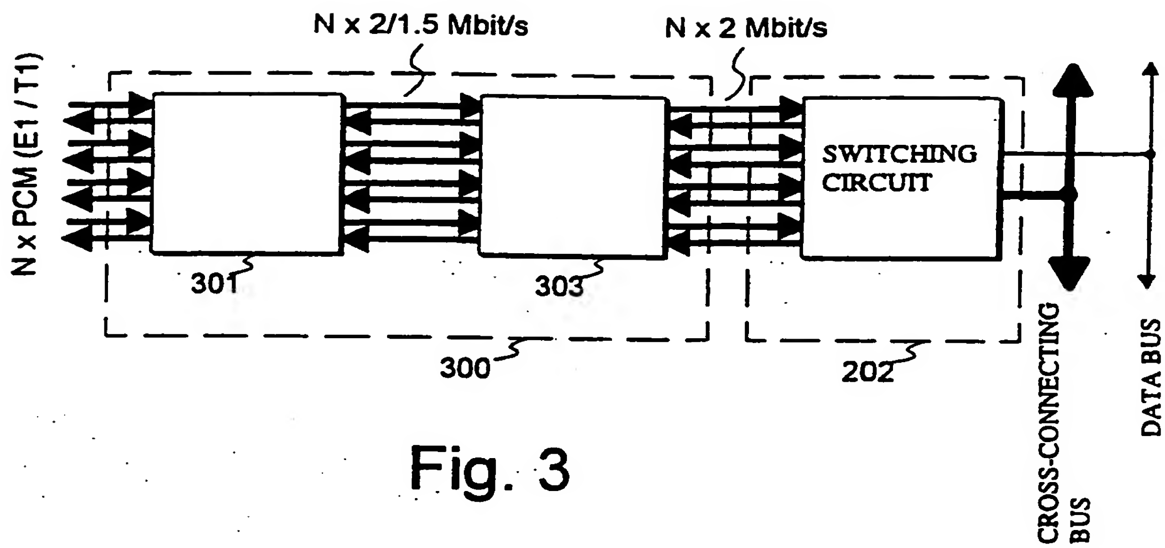
N x 2/1.5 Mbit/s
N x 2 Mbit/s
N x PCM (E1 / T1)
SWITCHING CIRCUIT
301
303
300
202
CROSS-CONNECTING BUS
DATA BUS

Fig. 3

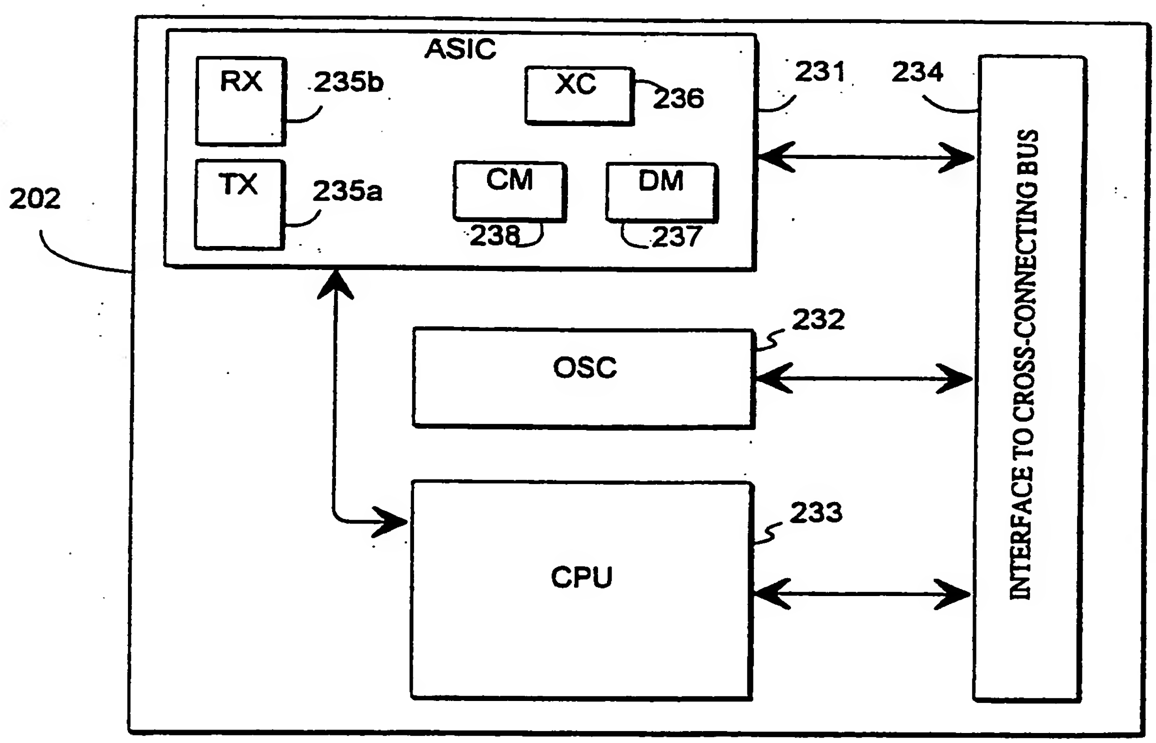
ASIC
RX
235b
TX
235a
XC
236
CM
238
DM
237
231
234
202
232
OSC
233
CPU
INTERFACE TO CROSS-CONNECTING BUS

Fig. 4

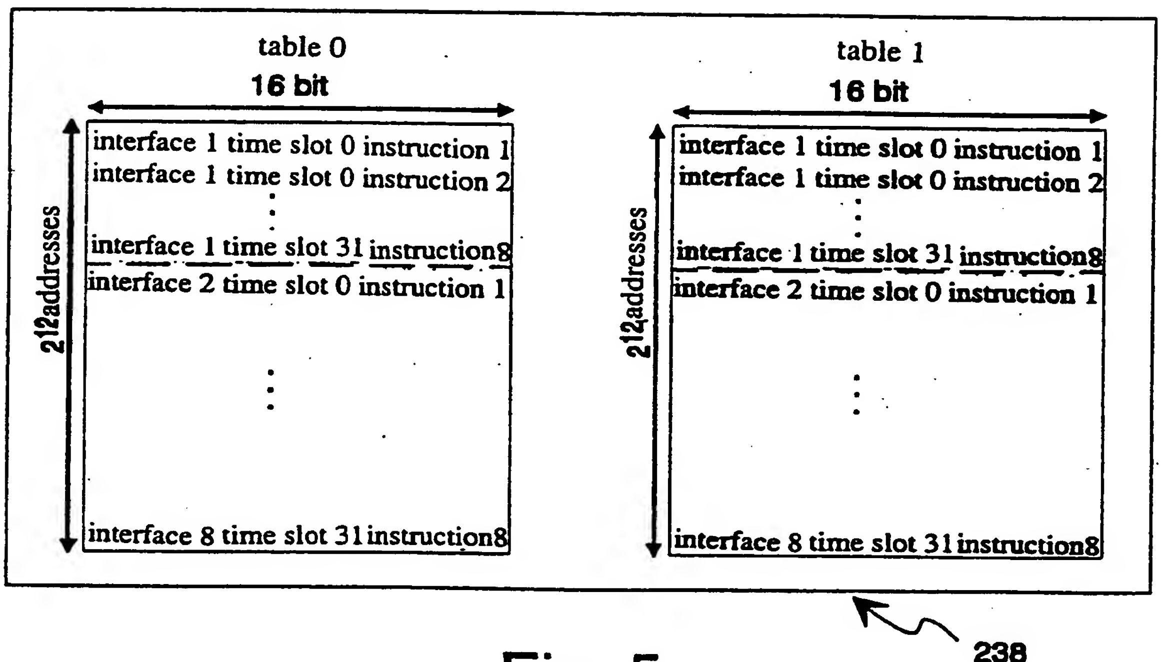
table 0
16 bit
2^12 addresses
interface 1 time slot 0 instruction 1
interface 1 time slot 0 instruction 2
interface 1 time slot 31 instruction8
interface 2 time slot 0 instruction 1
interface 8 time slot 31 instruction8
table 1
16 bit
2^12 addresses
interface 1 time slot 0 instruction 1
interface 1 time slot 0 instruction 2
interface 1 time slot 31 instruction8
interface 2 time slot 0 instruction 1
interface 8 time slot 31 instruction8
238

Fig. 5

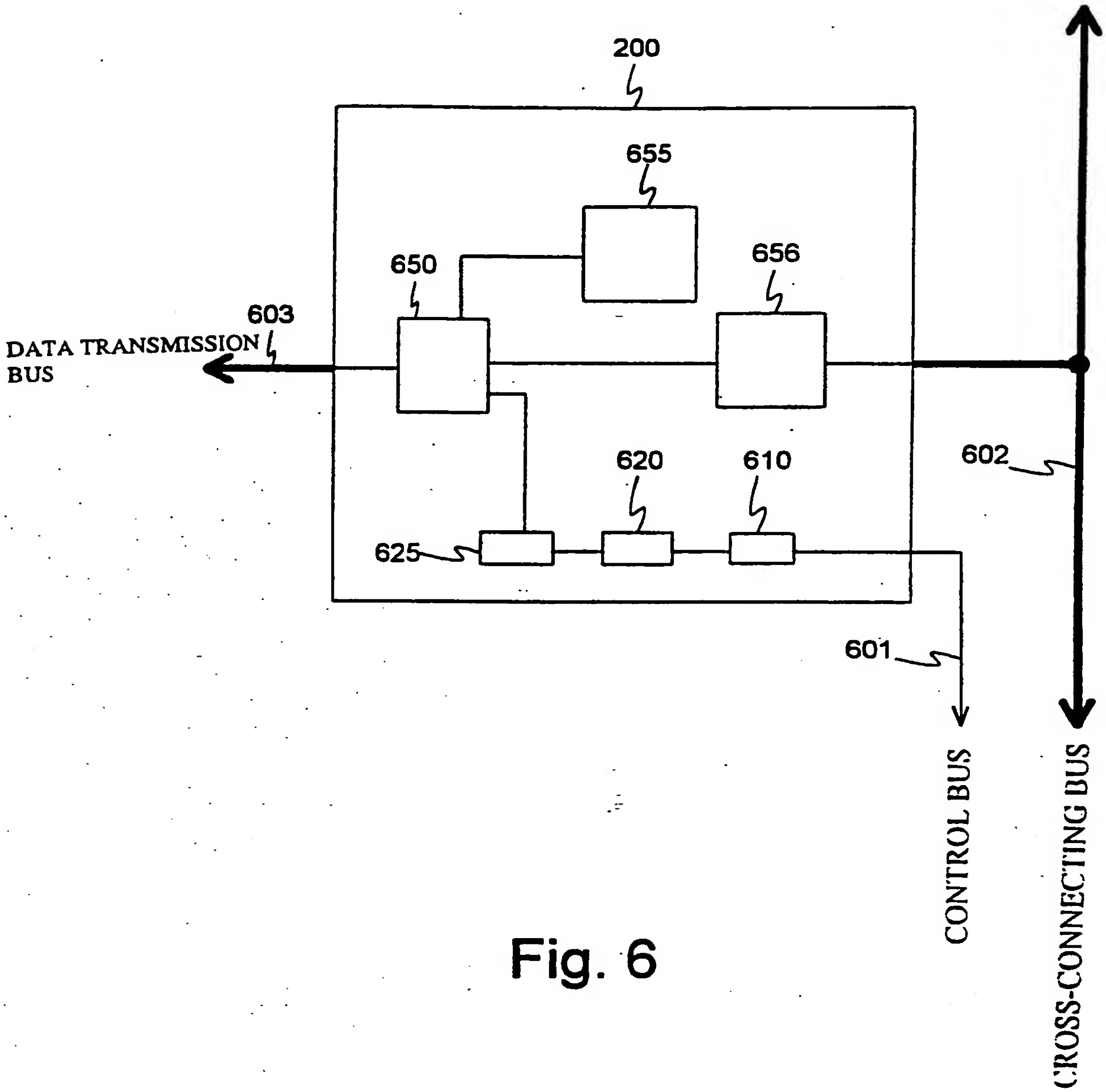
200
655
650
656
603
DATA TRANSMISSION BUS
620
610
602
625
601
CONTROL BUS
CROSS-CONNECTING BUS

Fig. 6

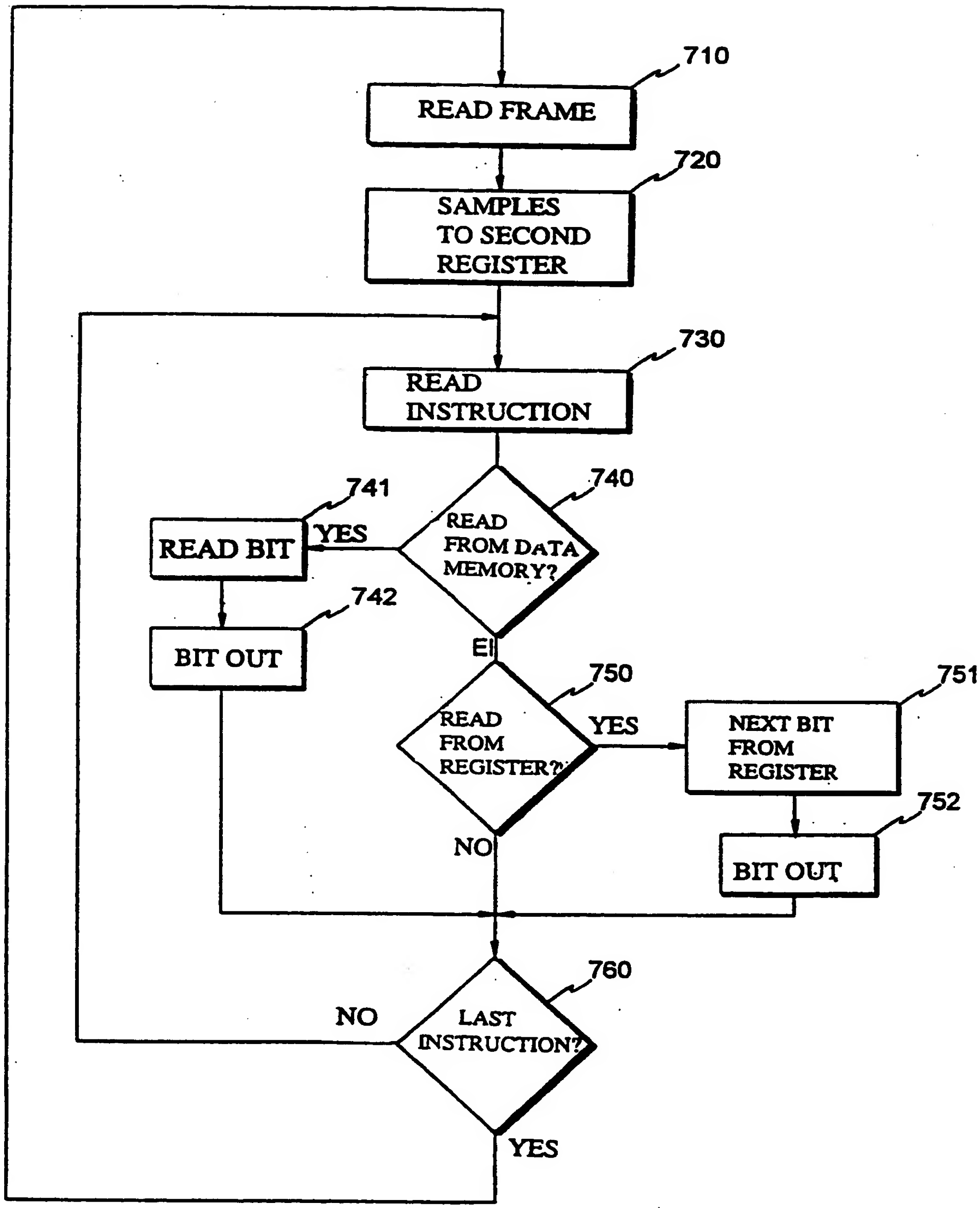
710
READ FRAME
720
SAMPLES TO SECOND REGISTER
730
READ INSTRUCTION
740
READ FROM DATA MEMORY?
741
YES
READ BIT
742
BIT OUT
EI
750
READ FROM REGISTER?
YES
751
NEXT BIT FROM REGISTER
752
BIT OUT
NO
760
NO
LAST INSTRUCTION?
YES

Fig. 7

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